ECE 627 Project: Design of a High-Speed Delta-Sigma A/D Converter

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I. Introduction

The goal of the Spring 2008, ECE 627 project is to design a complete switched-capacitor (SC) delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC) including the switched-capacitor delta-sigma modulator and the digital decimation filter targeted toward a 1V, 90nm CMOS process. The design specifications are shown in Table I.

TABLE I
Design Specifications

Signal Bandwidth	$0 - 20$ MHz
Clock Frequency	≤ 640 MHz
Accuracy	≥ 11 bits
Power Supply	1 V

For this design, the signal-to-quantization noise ratio must be greater than $68dB$, where

$$SQNR = 20 \cdot \log_{10}\left(2^{ENOB}\right) + 20 \cdot \log_{10}\left(\sqrt{\frac{3}{2}}\right). \quad (1)$$

A. Modulator Order, Quantizer Levels, and Oversampling Ratio Trade-offs

The oversampling ratio (OSR) can be at most $F_S/(2 \cdot F_{BW}) = 16$. After examining the empirical SQNR limit versus OSR and modulator order [1], I saw that a single bit quantizer cannot meet the design specification, which leads me to consider a multi-bit quantizer. I chose to use a third order modulator with a 9-level quantizer, which can obtain at most 85dB SQNR. Considering SQNR degradation due to thermal noise and non-ideal amplifier characteristics, among others, the actual SQNR performance will be worse. The use of a multi-bit quantizer can increase the stability in high order modulators, and the odd number of quantizer levels in this design simplifies the design of the feedback digital-to-analog converter (DAC).

Another option would be to use a fifth order modulator with 3-bit quantizer with an OSR of 8 to provide at most 78dB SQNR. The lower OSR allows the sampling frequency to be reduced to 320 MHz which will reduce dynamic power consumption at the expense of higher static power consumption in the two additional switched capacitor integrators. I believe that the additional complexity of a fifth order modulator is not required since in a deep sub-micron process, dynamic power consumption is not necessarily dominant.

B. Modulator Architecture Comparison

The four most common modulator architectures [2] are

- Cascade-of-integrators, feedback form (CIFB)
- Cascade-of-integrators, feedforward form (CIFF)
- Cascade-of-resonators, feedback form (CRFB)
- Cascade-of-resonators, feedforward form (CRFF).

The CIFB and CIFF architectures use delaying integrators for all states, whereas CRFB and CRFF architectures use both delaying and non-delaying integrators. All architectures can implement optimized noise transfer function (NTF) zeros, but only the CRFB and CRFF architectures can place optimized NTF zeros directly on the unit circle for maximum SQNR improvement. The non-delaying integrators used in CRFB and CRFF structures lead to increased amplifier slew-rate and bandwidth requirements.

Traditional feedback architectures stabilize the modulator by feeding back the modulator output to each integrator. The feedforward architecture, also known as the low-distortion architecture [3], sums all integrator outputs and the input signal at the input of the quantizer. Ideally, no signal information is passed through the integrators. The feedforward architecture has the benefits of low signal distortion and only one feedback DAC, with the drawback of an extra amplifier to accurately sum the input and integrator outputs. The feedback architecture has the benefits of lower power at the expense of higher signal distortion and the complexity of multiple feedback DACs.

C. Modulator Architecture Summary

I chose to implement the analog modulator as a third order CIFF with 9-level quantizer and optimized zero placement (Fig. 1). With the NTF zeros not on the unit circle, the resulting loss in SQNR is $< 1dB$. The additional summing amplifier does not significantly impact the SQNR because it is shaped by a third order high-pass transfer function.

II. Theoretical Design

The modulator shown in Fig. 1 has signal transfer function (STF) and noise transfer function

$$STF(z) = 1 \quad (2)$$

$$NTF(z) = \left(1 - z^{-1}\right)^3. \quad (3)$$

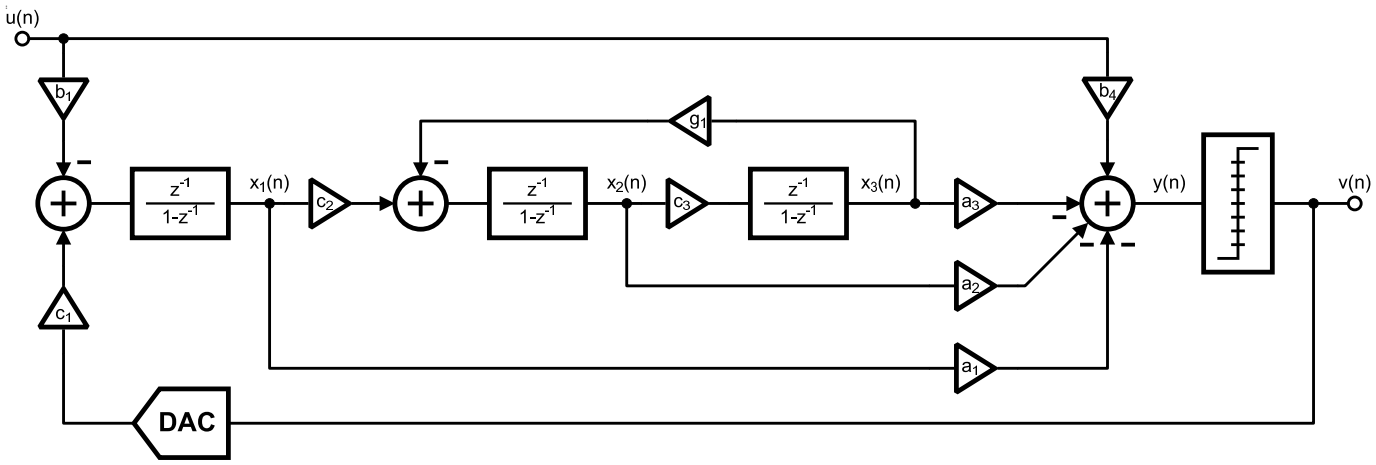

Fig. 1. Third order delta-sigma modulator with 9-level quantizer

Both (2) and (3) were found by setting $g_1 = 0$ and choosing a_i, b_i, and c_i to set $STF = 1$ and $NTF = (1 - z^{-1})^3$. From this starting point, I used the Delta-Sigma Toolbox [2] to optimize the modulator coefficients (Table X). I found that the modulator was stable with $\|H\|_\infty < 8$, but I chose $\|H\|_\infty = 6.8$ and the maximum quantizer input amplitude to be $8/9 \cdot V_{REF}$ to maximize SQNR while maintaining a reasonable maximum stable input amplitude of $0.4 \cdot V_{REF}$. Figure 2 shows the NTF and STF magnitude response for the coefficients shown in Table II. The poles and zeros are shown in Fig. 3.

TABLE II
MODULATOR COEFFICIENTS

a_1	2.885522268923101
a_2	2.795275751639167
a_3	0.858455887399655
b_1	1
b_4	1
c_1	1
c_2	1
c_3	1
g_1	0.022954073145617

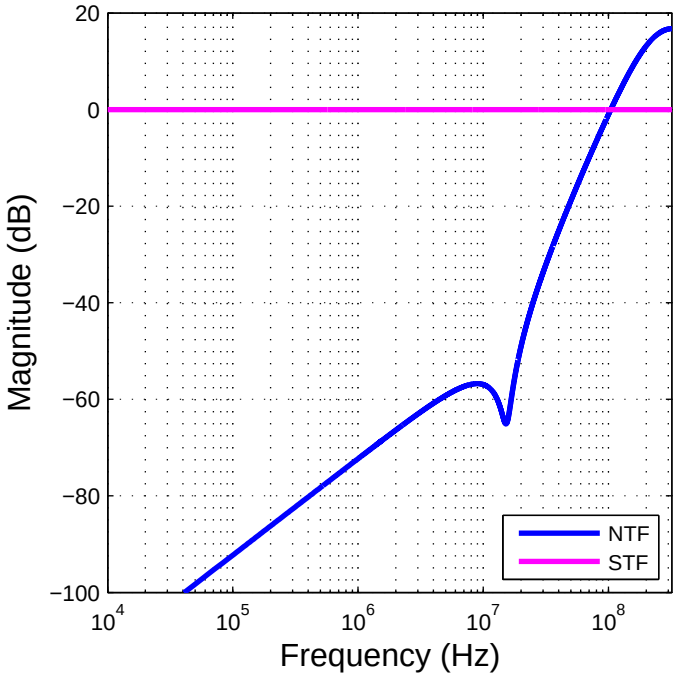

Fig. 2. Ideal NTF and STF magnitude response

Because the modulator architecture is CIFF, the two complex zeros do not lie exactly on the unit circle (Fig. 3). The signal transfer function is equal to one for all frequencies and has no poles or zeros.

The simulation results presented in Fig. 4 show that SNR degrades for higher frequencies. These simulations were run with both 2^{13} and 2^{16} points with little difference in results.

III. Dynamic Range Optimization

Dynamic range optimization of the integrator outputs $x_i(n)$ and quantizer input $y(n)$ can help minimize the affects of non-ideal circuit performance such as thermal noise and charge injection. The dynamic range scaling of $y(n)$ was discussed in Section II.

I carefully scaled the modulator coefficients allowing some margin for amplifier output swing, while constraining the final quantized coefficients to be mostly integer fractions. The unscaled and scaled integrator outputs, normalized to V_{REF}, are shown in Fig. 5.

To allow greater input flexibility, I decided to use ground and V_{DD} as the DAC references and allow the input signals to span the entire 1V power supply range. Since the amplifiers would only allow approximately $\pm 0.5 V_{diff}$ swing, the b_1, b_4, and c_1 coefficients must be scaled by $1/2$. In addition, the b_i coefficients must be scaled by $2/5$ to accommodate the rail-to-rail input voltage and not allow the modulator to go unstable.

The final full precision and quantized coefficients are shown in Table III. Note that the g_1 coefficient was quantized to $1/60$

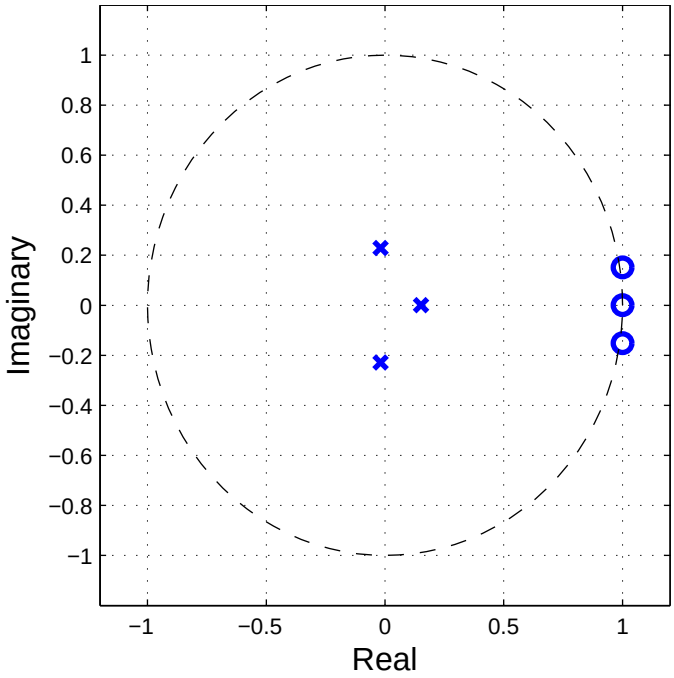

Fig. 3. Ideal NTF poles and zeros

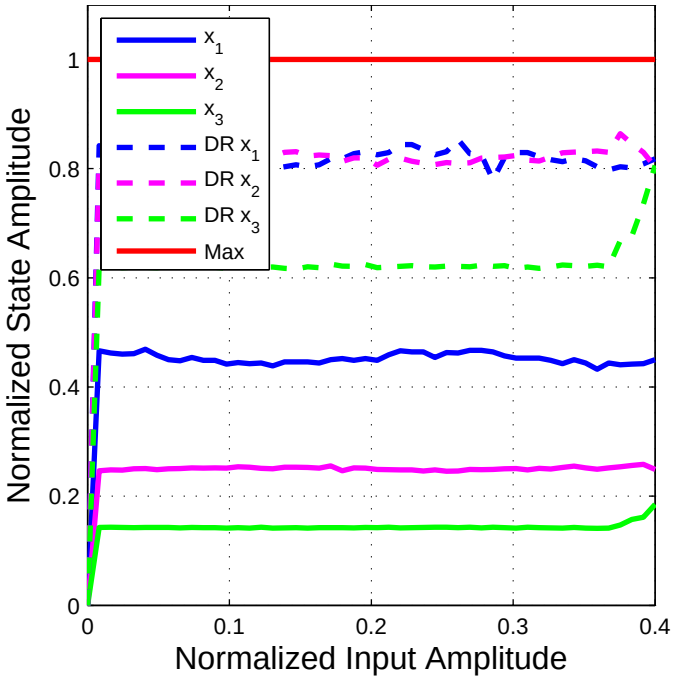

Fig. 5. Unscaled and dynamic range scaled normalized integrator outputs versus normalized input amplitude

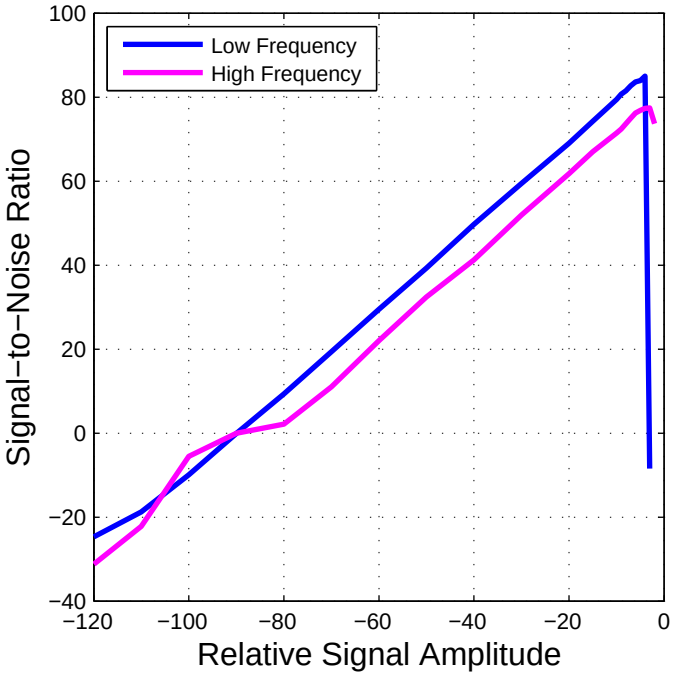

Fig. 4. Signal-to-noise ratio versus relative input amplitude for low and high frequencies

to take advantage of integer ratios of the second integrator, and minimize total capacitance. Differences between full precision and quantized modulator coefficients have not significantly impacted SQNR performance.

TABLE III
DYNAMIC RANGE SCALED MODULATOR COEFFICIENTS

	Full Precision	Quantized
a_1	1.587037247907706	17/11
a_2	0.854112035223079	9/11
a_3	0.196729474195754	2/11
b_1	0.363636363636364	8/22
b_4	0.2	2.2/11
c_1	0.909090909090909	20/22
c_2	1.8	9/5
c_3	1.333333333333333	4/3
g_1	0.017215554859213	1/60

IV. SWITCHED-CAPACITOR IMPLEMENTATION

To begin the ideal switched-capacitor circuit design, I carefully constructed the clock timing diagram shown in Fig. 6 by examining the system block diagram (Fig. 1).

The switch-capacitor adder (Fig. 7) and switched-capacitor integrators (Fig. 8) circuit diagrams follow directly the timing shown in Fig. 6. Note that the modulator utilizes fully differential circuits, and the circuit diagrams are drawn single ended for clarity. The quantizer is modeled as a 9-level flash ADC. The transient state voltages are show in Fig. 9.

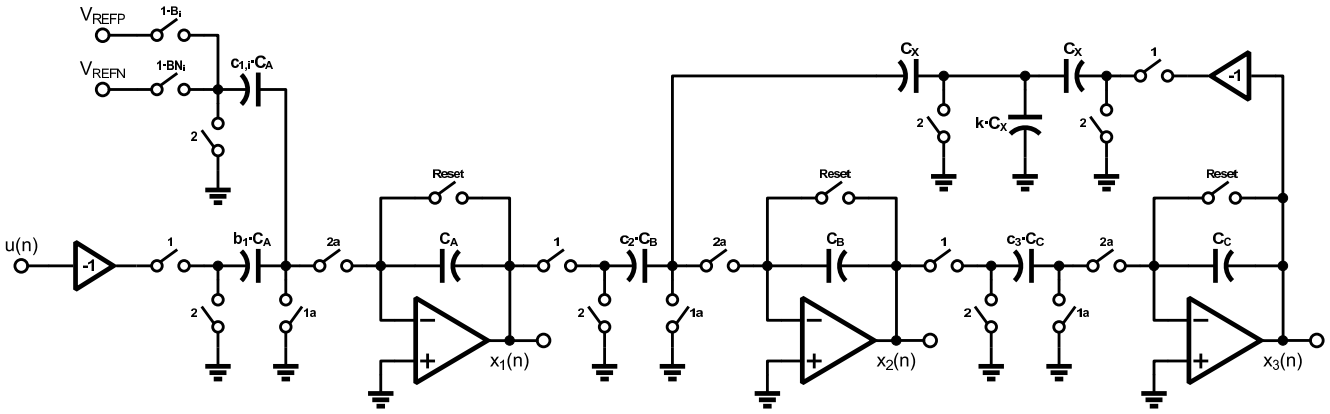

Fig. 8. Switched-capacitor integrators circuit diagram portion of modulator

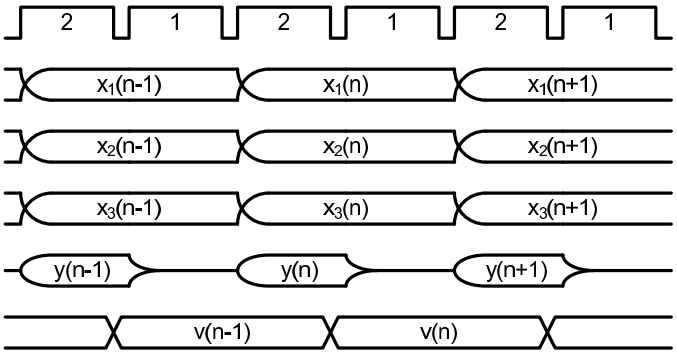

Fig. 6. Switched-capacitor modulator clock timing diagram

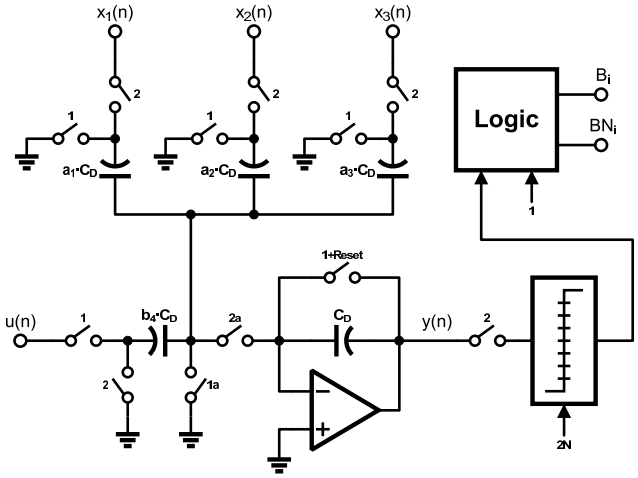

Fig. 7. Switched-capacitor add circuit and quantizer diagram portion of modulator

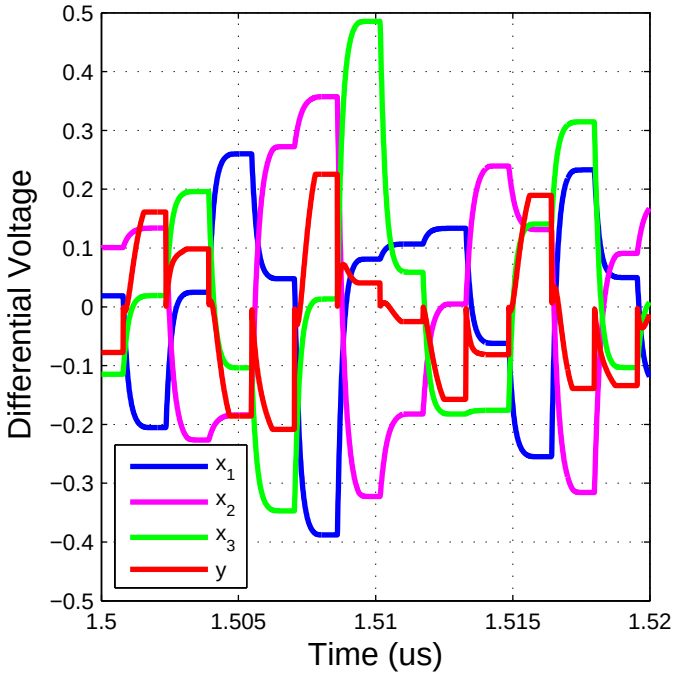

Fig. 9. Switched-capacitor transient simulation results

A. kT/C Thermal Noise

The in-band thermal noise due to the sampling capacitors $b_1 \cdot C_A$ and $c_1 \cdot C_A$ is given by

$$SNR = 10 \cdot \log_{10} \left(\frac{\frac{1}{2} V_{IN}^2 \cdot OSR}{\frac{4kT}{C_A} \left(\frac{1}{b_1} + \frac{1}{c_1} \right)} \right) \quad (4)$$

A reasonable value for C_A is $660fF$ and results in an in-band thermal noise SNR of 76.2dB. The addition of in-band quantization noise and non-ideal circuit errors of the first integrator will further reduce the SQNR. The thermal noise from the second integrator can be ignored if it is within 4 to 5 times higher than the first integrator's thermal noise. The is because the second integrator's noise is input referred back through the first integrator, which shapes it with a first order high-pass transfer function. In-band noise from succeeding stages is further suppressed.

B. Slew Rate and Gain Bandwidth

To determine the slew rates of each state, x_i and y, when the amplifiers are allowed to slew for 20% of T_S, I used the following equation.

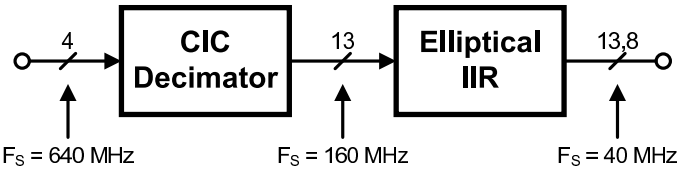

Fig. 10. Digital decimation filter block diagram

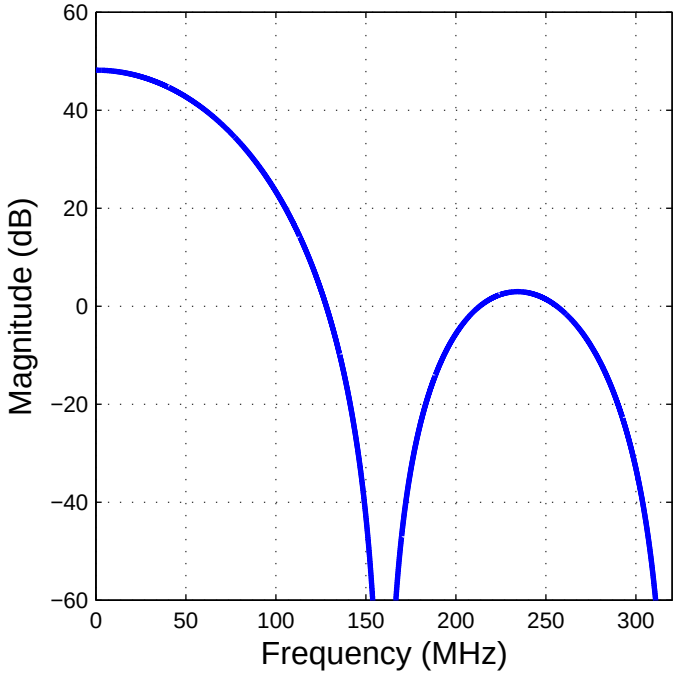

Fig. 11. Magnitude response of a fourth order CIC decimation filter with internal downsample by 4

$$SR(x) = \frac{\max|x(n) - x(n-1)|}{0.2 \cdot T_S/2} \tag{5}$$

I found that all states had a maximum slew rate of $4.8V/ns$ to $5.2V/ns$. Through further simulations, I determined the amplifier closed-loop bandwidth should be approximately 2 times the sampling clock frequency.

V. Decimation Filter Design

The decimation filter design is composed of two digital filters (Fig. 10). The first is a fourth order cascaded integrator-comb (CIC) FIR decimation filter (Fig. 11), down-sampled by 4 [4]. The CIC decimation filter is an efficient digital filter constructed of cascaded digital integrators followed by down-sampler followed by cascaded digital differentiators. It is common knowledge that the CIC filter should have an order one higher than the modulator order to minimize folded in-band quantization noise, and should down-sample to rate of $8 * F_{BW}$ to minimize in-band signal attenuation at frequencies close to F_{BW}.

The second filter is a ninth order (9w) elliptical IIR filter (Fig. 12) with passband ripple of $0.1dB$ and stop-band attenuation of $111dB$, which places zeros at $40MHz$ and $80MHz$ to minimize folded in-band quantization noise when down-sampled to baseband.

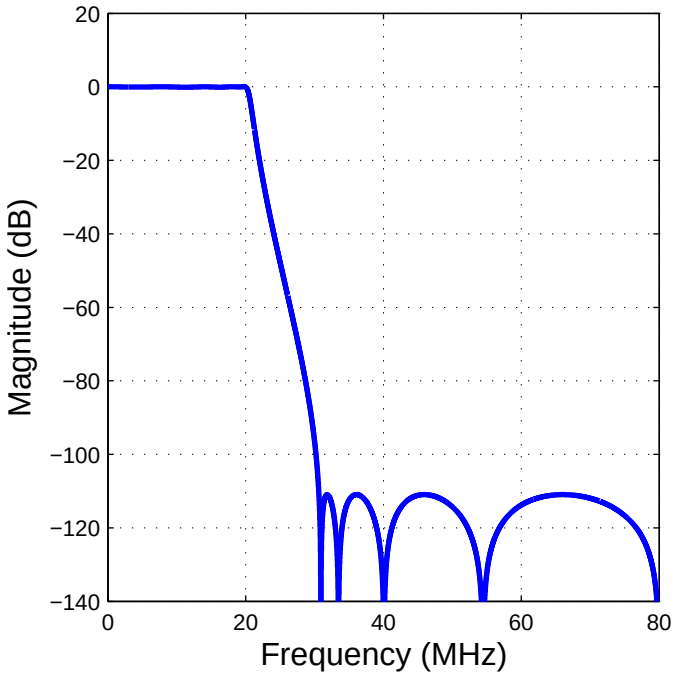

Fig. 12. Magnitude response of a ninth order elliptical IIR filter

Using these filters, the total in-band signal attenuation due to digital filtering is $< 1dB$.

VI. Performance Analysis Using MATLAB/Simulink

I utilized the numerical power of MATLAB/Simulink to simulate the non-ideal affects of finite amplifier gain, amplifier slew rate, amplifier gain bandwidth, amplifier thermal noise, capacitor mismatch in the feedback DAC, and digital filter round-off error [5]. All simulation results are the average of 32 uncorrelated runs [6].

A. Finite Gain

Amplifier finite gain causes a shift in the NTF zeros from $z = 1$ to a point inside the unit circle [7]. This causes an increase in the noise floor, and may introduce distortion tones. Since the feedback factor is close to 1, the amplifier open-loop gain [7] should be

$$A_0 \gg \frac{OSR}{\pi} - 2 \tag{6}$$

Fig. 13 shows the modulator output spectrum for $A_0 = 10, 100, 1000V/V$. Choosing $A_0 = 10V/V$ does not satisfy (6), has large amplitude distortion tones, and reduces SNR by $8.5dB$ versus $A_0 = 100$. For this design, I chose $A_0 = 100$.

B. Finite Slew Rate

Amplifier slew rate can cause the output states to not completely reach their intended values. Like finite gain error,

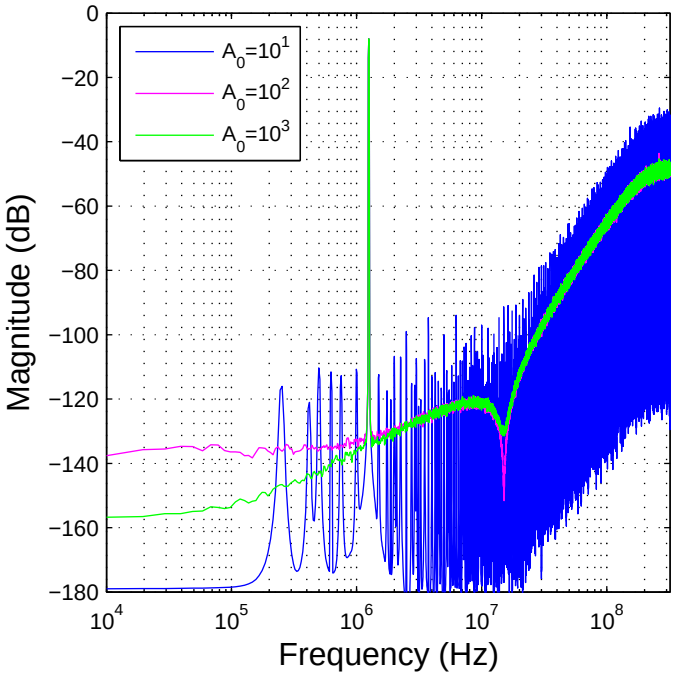

Fig. 13. Modulator output spectrum for $A_0 = 10, 100$, and $100V/V$

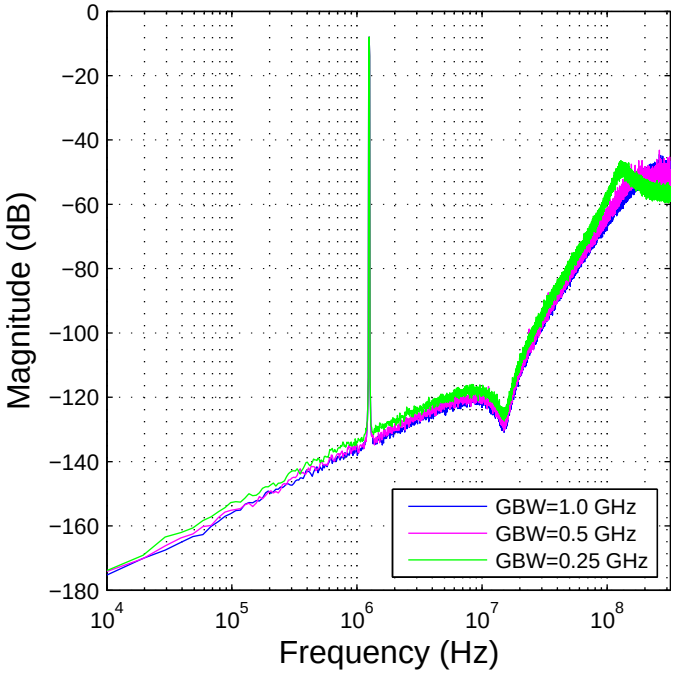

Fig. 15. Modulator output spectrum for $GBW = 0.25, 0.5$, and $1.0GHz$

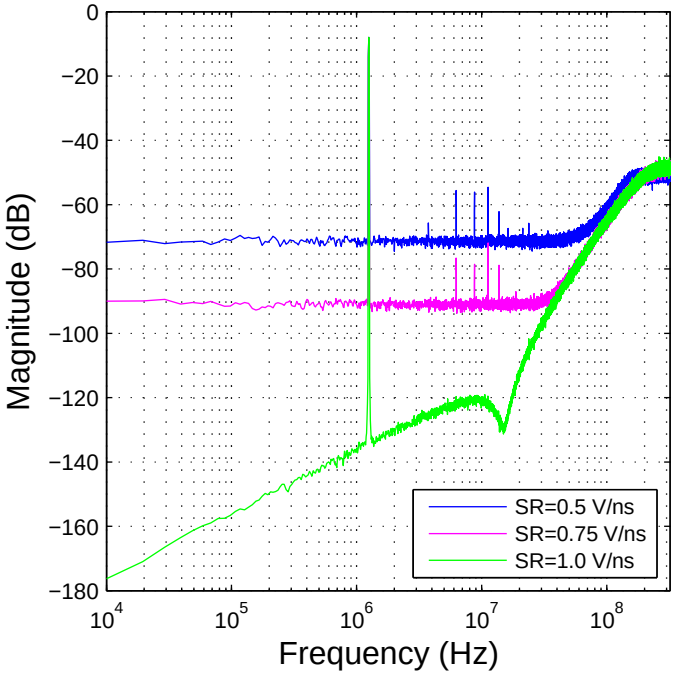

Fig. 14. Modulator output spectrum for $SR = 0.5, 0.75$, and $1.0V/ns$

limited slew rate results in an increase noise floor, but is more abrupt in its effect.

Fig. 14 shows the effect slew rate on the modulator output spectrum. This design uses slew rates of $4.8V/ns$ to $5.2V/ns$ to allow $< 0.2 \cdot T_S$ for slewing.

C. Finite Gain Bandwidth

Amplifier finite gain bandwidth effects are not as severe as the finite gain and slew rate effects. As the gain bandwidth decreases below the modulator sampling frequency, more of the out of band quantization noise is allowed to fold into the pass band (Fig. 15). Gain bandwidths of 1 to 2 times the sampling frequency are sufficient to meet the 11 bit accuracy requirements. For this design, I chose the GBW to be 1 GHz.

D. Amplifier Thermal Noise

To minimize the impact of amplifier input referred voltage noise should be limited to less than half the kT/C noise power from the sampling capacitors. The resulting thermal noise should be less than $35\mu V_{RMS}$.

$$v_{n,amp} \leq \frac{\sqrt{0.5 \cdot v_{n,kT/C}^2}}{1 + (1 + c_1)/b_1} \tag{7}$$

E. DAC Capacitor Mismatch and Dynamic Element Matching

Multi-bit feedback DACs work to increase modulator SQNR, but also suffer from non-linearities which generate in-band thermal noise and tones and limit SQNR. Data-weighted averaging (DWA), a type of element mismatch error shaping, was proposed [8] to high pass filter the DAC non-linearities. This method can suffer from idle tones under certain conditions. Fig. 16 shows that DAC with 8-bit 1-σ

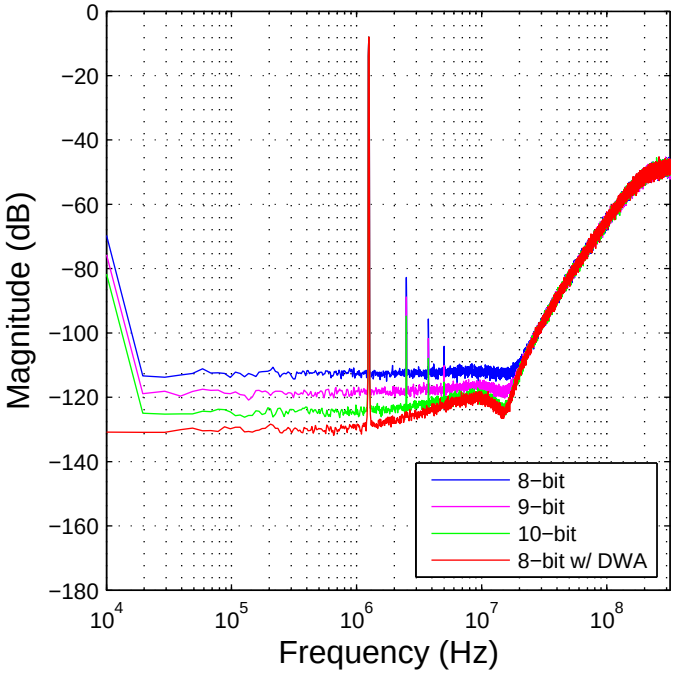

Fig. 16. Modulator output spectrum for DAC capacitor mismatch of 8, 9, 10-bit, and 8-bit with DWA

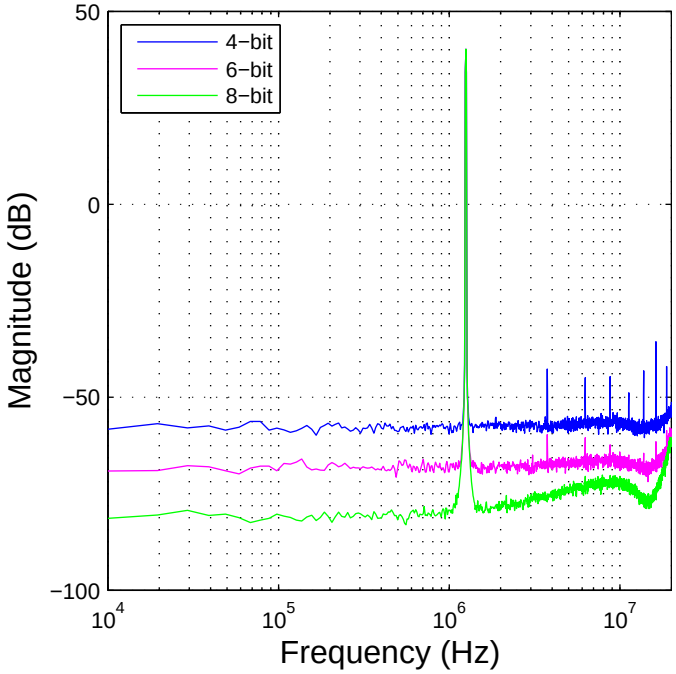

Fig. 17. ADC output spectrum for 4, 6, 8-bit IIR filter fraction lengths

matching can have a lower noise floor without the harmonic distortion than a 10-bit 1-σ matched DAC.

Because this modulator uses the CIFF architecture, capacitor mismatch between b_1, b_4, and c_1 terms will lead to an STF that is not 1 for all frequencies. Significant mismatches in all coefficients could lead to internal state saturation and distortion.

F. Digital Filter Round-off Effects

The digital filtering of the modulator stream is an important component in overall ADC performance. Quantization of filter coefficients and fractional precision can result in spurious tones in the digital baseband signal.

The CIC decimation filter can be minimized [4] by optimizing individual register lengths based on the input and output word lengths.

The IIR filter is sensitive to coefficient quantization and fractional residue of internal states and the output word. Since IIR input word easily occupies a 13-bit space and the IIR filter peak gain is 0.1dB, the IIR output word length may remain 13-bits. However, the output fraction length will greatly influence the complete ADC SNR performance. Fig. 17 shows the ADC output spectrum for several output fraction lengths. For this design, I chose an 8-bit fraction length for a total 21-bit output word.

VII. Conclusion

Table IV summarizes the design parameters and results of this ADC. The modulator (Fig. 18) and ADC (Fig. 19) output spectrum show results of simulations with all considered noise sources (kT/C noise, finite amplifier gain, amplifier slew rate, amplifier gain bandwidth, amplifier thermal noise, capacitor mismatch in feedback DAC, and digital filter quantization).

TABLE IV
Design Specifications

Signal Bandwidth	$0 - 20$ MHz
Clock Frequency	≤ 640 MHz
Min Unit Cap	25 fF
Total Capacitance	6.71 pF
Amplifier DC Gain	100 V/V
Amplifier SR	5.2 V/ns
Amplifier GBW	1.0 GHz
DAC 1-σ	0.39%
Total Word Length	21 bits
Fraction Length	8 bits
ENOB @ 156.25 kHz	11.69 bits
ENOB @ 20 MHz	11.36 bits
Power Supply	1V
Input Signal Range	$\pm 1 V_{diff}$

Acknowledgment

The author would like to thank Sunwoo Kwon and Prof. Pavan Kumar Hanumolu for their discussions on delta-sigma modulators.

References

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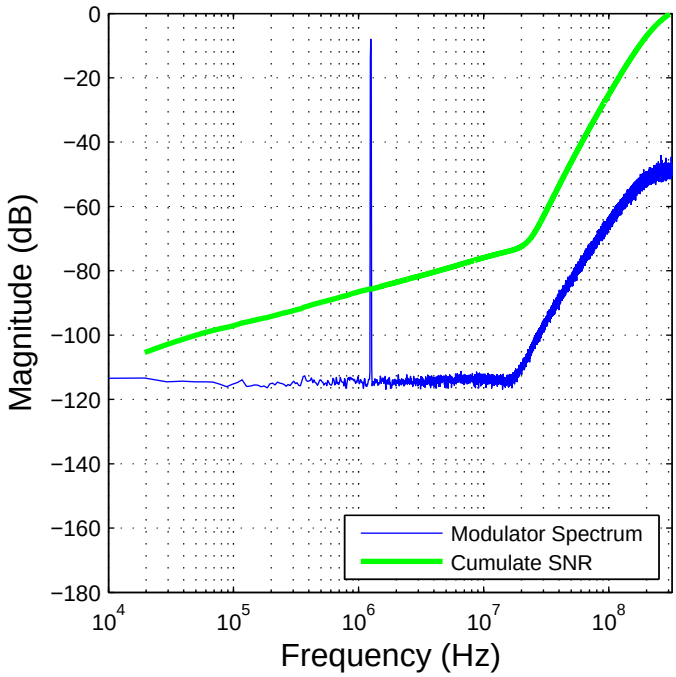

Fig. 18. Modulator spectrum and cumulative SNR for 1.25 MHz full-scale input

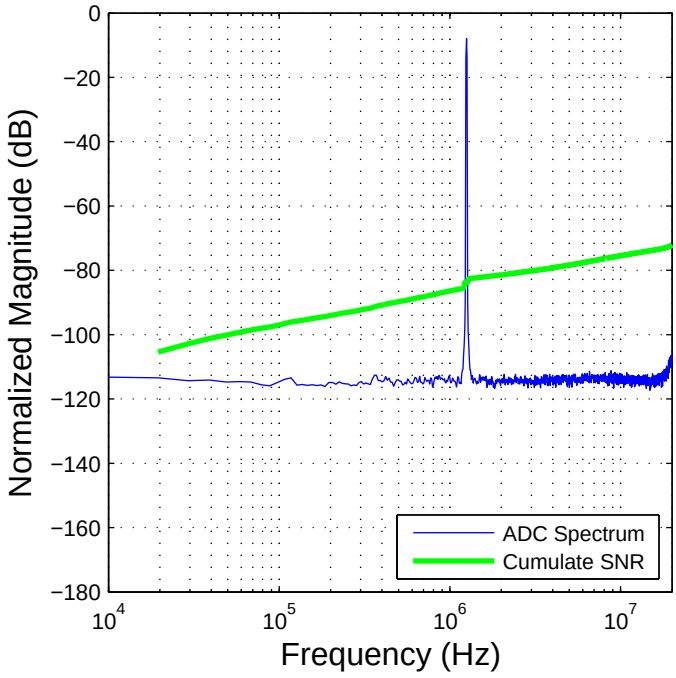

Fig. 19. ADC spectrum and cumulative SNR for 1.25 MHz full-scale input

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APPENDIX A
CADENCE DATABASE

This section contains all Cadence circuit level simulation files for this design.

APPENDIX B
MATLAB/SIMULINK DATABASE

This section contains all MATLAB/Simulink scripts and model files for this design.